10/623149 01-14-05

copy/~~46~~

Express Mail Label No. Dated: ______________

Docket No.: 08211/0200245-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Bumha Lee et al.

Patent No.: 6,791,484

Issued: September 14, 2004

For: METHOD AND APPARATUS OF SYSTEM OFFSET CALIBRATION WITH OVERRANGING ADC

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322 AND 37 CFR 1.323

MS Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted and error which should be corrected.

In the Application:

Column 2, Line 18, Delete "EMBODIMENTS" and insert -- EMBODIMENT--.

Column 2, Line 59, After "overrange" delete ",".

Column 4, Line 7, Delete "2^{10-1}" and insert - - 2^{10}-1 - -.

Column 4, Line 14 Delete "in any" and insert -- many--.

Column 4, Line 25 After "D_out" delete ",".

Column 4, Line 65 After "reference" delete ",".

Column 5, Line 31, Delete "(Q_h)," and insert - - (Q_h). - -.

Column 5, Line 47, After "see" delete ".".

Column 6, Line 31, Delete "1100" and insert - - 1110 - -.

Column 6, Line 43, Delete "since" and insert - - . Since - -.

Column 10, Line 31, In Claim 19, delete "con figured" and insert - - configured - -.

The following errors were found in the application as filed by applicant. The errors now sought to be corrected are inadvertent typographical errors, the correction of which does not involve new matter or reexamination.

Column 4 Line 38-39, Delete "analog-to-digital-conversion" and insert - - analog-to-digital conversion - -.

Column 7, Line 8, In Claim 2, delete "course" and insert - - coarse - -.

Column 9, Line 41, In Claim 15, after "response" insert - - to - -.

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find a check for $100.00 and copies of pages 3, 5, 6, 7, 8, 10, 11, 15 & 16 of the application as filed.

JAN 2 5 2005

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: January 11, 2005

Respectfully submitted,

By ______________________

Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 753-6237 (Fax)
Attorneys/Agents For Applicant

JAN 25 2005

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,484

DATED : September 14, 2004

INVENTOR(S) : Bumha Lee et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Application:

Column 2, Line 18, Delete "EMBODIMENTS" and insert -- EMBODIMENT--.
Column 2, Line 59, After "overrange" delete ",".
Column 4, Line 7, Delete "2^{10-1}" and insert - - 2^{10}-1 - -.
Column 4, Line 14 Delete "in any" and insert -- many--.
Column 4, Line 25 After "D_out" delete ",".
Column 4, Line 65 After "reference" delete ",".
Column 4 Line 38-39, Delete "analog-to-digital-conversion" and insert - - analog-to-digital conversion - -.
Column 5, Line 31, Delete "(Q_h)," and insert - - (Q_h). - -.
Column 5, Line 47, After "see" delete ".".
Column 6, Line 31, Delete "1100" and insert - - 1110 - -.
Column 6, Line 43, Delete "since" and insert - - . Since - -.
Column 7, Line 8, In Claim 2, delete "course" and insert - - coarse - -.
Column 9, Line 41, In Claim 15, after "response" insert - - to - -.
Column 10, Line 31, In Claim 19, delete "con figured" and insert - - configured - -.

MAILING ADDRESS OF SENDER:
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

PATENT NO. 6,791,484

No. of additional copies 1

JAN 2 5 2005

Figure 10 is a graphical illustration of a residue curve for an example embodiment of an MDAC that is configured for operation in the ADC system of Figure 3.

Figure 11 illustrates another example embodiment of an overranging ADC that is arranged for operation the ADC system of Figure 3.

Detailed Description of the Preferred Embodiment

Throughout the specification and claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal. Referring to the drawings, like numbers indicate like parts throughout the views.

Briefly stated, the invention is related to a method and apparatus for system offset calibration using an overranging ADC. The overranging ADC is configured to convert an analog signal into an intermediary digital signal. The conversion range of the overranging ADC is extended beyond the full dynamic range of the ADC system. The intermediary digital signal has more bits than the digital output signal. A digital fine offset adjustment circuit is configured to provide the digital output signal by digitally subtracting a fine offset from the intermediary digital signal and decoding the intermediary digital signal. The digital output signal has approximately no offset, and has approximately no loss in dynamic range.

DAC_control into an analog signal that is provided at node N342. Summer block 310 is configured to provide a signal at node N340 in response to signal IN and the signal at node N342. Summer circuit 310 is arranged to provide the signal at node N340 such that the voltage at node N340 corresponds to the sum of the voltages at node N330 and N342. PGA block 314 is configured to amplify or attenuate the signal at node N340 to provide signal A_in at node N320.

Operation of Overranging ADC

Overranging ADC 306 is arranged to convert A_in into an intermediary digital signal (D_out), where D_out is provided at node N322. Overranging ADC 306 may be implemented by a variety of different architectures, including a pipeline analog-to-digital conversion architecture, and a flash analog-to-digital conversion architecture. The output range of overranging ADC 306 extends beyond the full dynamic range (FDR) of system 300.

Figure 4 is a graphic illustration for an output range of an example embodiment of an overranging ADC that is arranged in accordance with aspects of the present invention.

The full dynamic range (FDR) of system 300 extends from a first digital level (404) to a second digital level (406). Digital level 404 corresponds to a lower bound analog input voltage (e.g., V_{NEG}). Digital level 406 corresponds to an upper bound analog input voltage (e.g., V_{POS}). The output range of overranging ADC 306 extends from a third digital level (402) to a fourth digital level (408). Digital level 402 corresponds to a system lower bound analog input voltage (e.g. V_{LO}). Digital level 408 corresponds to a system upper bound analog input voltage (e.g. V_{HI}), where level 402 is less than level 404 relative to level 406, and level 408 is greater than level 406 relative to level 402. The output range of overranging ADC 306 includes the full dynamic range (FDR), a lower overrange from 402 to 404, and an upper overrange from 406 to 408. Part of signal D_out will be included in the lower overrange when the system offset is negative as illustrated by range 1. Part of signal D_out will be included in the upper overrange when the system offset is positive as illustrated by range 2.

Figure 5 is a graphic illustration for an output range for another example embodiment of an overranging ADC that is arranged in accordance with aspects of the present invention. According to the example illustrated in Figure 5, V_{LO} corresponds to $-5/4$ V, V_{NEG} corresponds to -1V, V_{POS} corresponds to 1V, and V_{HI} corresponds to 5/4 V, and the full dynamic range (FDR) of system 300 corresponds to 10 bits. The conversion range of overranging ADC 306 corresponds to 10.25 bits, where the overrange on each side is 1/8 of the full dynamic range (FDR). The 10-bit output range of system 300 extends from a digital code of 0 at level 404 to a digital code of 1023 (2^{10}-1) at level 406. The 10.25-bit conversion range of overranging ADC 306 extends from a digital code of 0 at level 402 to a digital code of 1279 ($2^{10}+2*2^{7}-1$) at level 408. For this example, an input voltage of V_{NEG} results in a digital output code of 128, while an input voltage of V_{POS} results in a digital output code of 1151. Although Figure 5 illustrates specific values (ranges and output codes), many other embodiments are considered within the scope of the present invention.

<u>Operation of Digital Control Block</u>

Coarse offset calibration circuit 304 includes feedback logic for adjusting coarse DAC block 312. Coarse offset calibration circuit 304 is arranged to provide signal DAC_control at node N326 in response to signal D_out.

Signal D_out corresponds to a conversion code that is associated with the sum of the reference signal and the system offset during a calibration phase. Digital fine offset adjustment circuit 308 is configured to store a value (the fine offset) that is associated with signal D_out during the calibration phase.

Digital fine offset adjustment circuit 308 is further configured to digitally subtract the fine offset from signal D_out. Digital fine offset adjustment circuit 308 is further configured to decode signal D_out such that signal ADC_OUT corresponds to the correct digital code corresponding to the full dynamic range. For the example shown in Figure 5, signal D_out is decoded such that V_{NEG} corresponds to a digital code of 0 rather than 128, and V_{POS} corresponds to a digital code of 1023 rather than 1151.

Overranging ADC Examples

Overranging ADC 306 may be implemented via pipeline analog-to-digital conversion, flash analog-to-digital-conversion, or other methods of analog-to-digital conversion.

Figure 6 is an illustration an example embodiment of an overranging ADC (600) that is arranged for operation in the ADC system of Figure 3. Overranging ADC 600 includes stage 1 (610), a plurality of subsequent stages (612), and a digital correction circuit (602). According to one example, overranging ADC 600 is a 10.25 bit overranging ADC, where stage 1 (610) is a 3.5 bit stage and each of the subsequent stages (612) is a 1.5 bit stage. According to this example, stage 1 includes a 3.5 bit flash ADC (620) and a 3.5 bit MDAC (622).

Stage 1 provides a digital signal (DOUT1) and a residue signal (Residue1) in response to an intermediate analog signal (VIN). Each of the subsequent stages (612) provides another digital signal in response to the residue signal from the previous phase. Digital correction circuit 602 provides a digital intermediary digital signal (D_out) in response to the digital signal from each of the stages (610 and 612) and the residue signal (Residue9) of the last stage.

Figure 7 is an illustration of an example embodiment of a 3.5 bit ADC (620) that is arranged for operation in the ADC system. ADC 620 includes a reference voltage generator circuit (710), eight comparators (720-727), and a decoder block (730). Reference voltage generator circuit 710 is configured to provide eight reference voltages. According to one example, the eight reference voltages correspond to 7/8 * V_{POS}, 5/8 * V_{POS}, 3/8 * V_{POS}, 1/8 * V_{POS}, -1/8 * V_{POS}, -3/8 * V_{POS}, -5/8 * V_{POS}, and -7/8 * V_{POS}. The comparators (720-727) are configured to compare signal VIN to each of the eight reference voltages. The eight reference voltages provide 9 voltage ranges. Decoder block 730 is configured to provide signal DOUT1 in response outputs of the comparators (720-727). Signal DOUT1 has a four-bit code that corresponds to the voltage range that signal VIN is within. Example digital codes and their associated voltage ranges are illustrated in Figure 9.

Figure 8A is an illustration of an example embodiment of an MDAC (622) that is configured for operation in the ADC system of Figure 3. MDAC 622 is a fully differential implementation. MDAC 622 includes eight sampling capacitors (C1-C8) (four on each signal path) and two feedback capacitors (CF1 and CF2) (one for each feedback path) that are arranged to operate with a fully differential operational transconductance amplifier such that a 3.5-bit conversion resolution is achieved.

Figure 8B is an illustration the example embodiment of MDAC 622 of Figure 8A during a sampling phase (Qs). The intermediate analog signal (VIN=INP-INN) is sampled on the sampling capacitors (C1-C8) during the sampling phase (Q_s). The top plate of each of the capacitors is coupled to a common mode level (CML). The bottom plate of each of the capacitors C1-C4 is coupled to signal INP, and the bottom place of each of the capacitors C5-C8 is coupled to signal INN. The feedback capacitors (CF1, CF2) are discharged. ADC 620 is configured to convert the intermediate analog signal (INP-INN) to a corresponding digital code at the end of the sampling phase (Q_s).

Figure 8C is an illustration of the example embodiment of MDAC 622 of Figure 8A during a holding phase (Q_h). During the holding phase (Q_h), MDAC 622 is arranged in a negative feedback configuration. MDAC 622 is arranged such that charges sampled on the sampling capacitors (C1-C8) are transferred to the feedback capacitors (CF1, CF2) during the holding phase (Q_h). The residue voltage (residue1=OUTP-OUTN) is scaled by the capacitance ratios. For example, MDAC 622 is configured to amplify the intermediate analog signal (INP-INN) by a transfer gain of four when each of the capacitors (C1-C8, CF1-CF2) has approximately the same capacitance rating. The gain factor may be adjusting by adjusting the capacitance of the capacitors (C1-C8, CF1-CF2).

The bottom plate of each of the sampling capacitors (C1-C8) is coupled to receive a reference voltage (VREF1-VREF8 respectively). Digital correction circuit 602 (see Figure 6) is configured to adjust the reference voltages (VREF1-VREF8) in response to signal DOUT1. The reference voltages (VREF1-VREF8) are determined by signal DOUT1. Example reference voltages are illustrated by Figure 9.

to the first reference signal (V_{NEG}) and the second reference signal (V_{POS}). Signal V_{HI} has a voltage that is greater than V_{POS}, and signal V_{LO} has a voltage that is less than V_{NEG}. V_{HI} and V_{LO} are provided as reference signal to the flash-type ADC (1110) such that the dynamic range of the flash-type ADC (1110) is extended beyond the normal reference range (i.e., V_{POS} and V_{NEG}).

Digital fine offset adjustment circuit 308 is configured to provide signal ADC_out with N bits of resolution. Flash ADC 1110 has a conversion range from V_{LO} to V_{HI}. Flash ADC 1110 is configured to convert signal A_in to signal Dout with N+X bits of resolution, where X is greater than 0. X corresponds to the additional resolution bits that are associated with the overranging operation of the flash-type ADC (1110).

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

What is claimed is:

1. An analog-to-digital converter system that is configured to provide a digital output signal in response to an analog input signal, the system comprising:

an overranging analog-to-digital converter that is arranged to convert an intermediary analog signal into an intermediary digital signal, wherein: the intermediary analog signal is related to the analog input signal, an output range associated with the overranging analog-to-digital converter extends beyond a full dynamic range of the analog-to-digital converter system, the intermediary digital signal has a first number of bits of resolution; and

a digital fine offset adjustment circuit that is configured to determine a fine offset during a calibration phase, and further configured to process the intermediary digital signal during a conversion phase such that: the determined fine offset is digitally subtracted from the intermediary digital signal to provide an offset adjusted digital signal, and the offset adjusted digital signal is decoded to provide the digital output signal such that the digital output signal has a second number of bits of resolution, wherein the first number of bits of resolution is greater than the second number of bits of resolution.

2. The analog-to-digital converter system of Claim 1 further comprising:

a coarse offset calibration circuit that is configured to adjust a course calibration control signal in response to the intermediary digital signal during the calibration phase; and

a coarse correction circuit that is arranged to perform coarse correction on the analog input signal to provide the intermediary analog signal, wherein the coarse correction circuit is responsive to the coarse calibration control signal.

3. The analog-to-digital converter system of Claim 2, wherein the coarse correction circuit is configured to provide coarse offset adjustment and the digital fine offset adjustment circuit is configured to provide fine offset calibration such that the digital output signal has approximately no offset.

voltage range of the intermediary analog signal approximately corresponds to the full dynamic range.

14. The method of Claim 11, wherein the output range of the intermediate digital signal includes a lower overrange and an upper overrange.

15. A analog-to-digital converter system that is configured to provide a digital output signal in response to an analog input signal, the system comprising:

a first means for converting that is arranged to convert an intermediary analog signal into an intermediary digital signal, wherein the intermediary analog signal is related to the analog input signal, an output range of the means for converting extends beyond a full dynamic range of the analog-to-digital converter system, the intermediary digital signal has a first number of bits of resolution, the digital output signal has a second number of bits of resolution, and wherein the first number of bits of resolution is greater than the second number of bits of resolution;

a means for determining that is configured to determine a fine offset in response to the intermediate digital signal during a calibration phase; and

a means for subtraction that is configured to digitally subtract the fine offset from the intermediary digital signal to provide an offset adjusted digital signal, wherein the offset adjusted digital signal corresponds to an offset adjusted version of the intermediate digital signal.

16. The analog-to-digital converter system of Claim 15, further comprising:

a means for correcting that is arranged to perform coarse correction on the analog input signal to provide the intermediary analog signal, wherein the means for correcting is responsive to a coarse calibration control signal; and

a second means for providing that is configured to provide the coarse calibration control signal in response the intermediate digital signal;

wherein the means for correcting comprises:

a second means for converting that is configured to convert the coarse calibration control signal into a coarse analog signal;

a means for summing that is configured to produce a sum signal in response to the analog input signal and the coarse analog signal, wherein the sum signal corresponds to a sum of the analog input signal and the coarse analog signal such that the sum signal corresponds to an offset corrected version of the analog input signal; and

a means for scaling that is configured to scale the sum signal according to a gain factor to provide the intermediary analog signal, wherein the gain factor is selected such that a voltage range of the intermediary analog signal approximately corresponds to the full dynamic range.

17. The analog-to-digital converter system of Claim 15, further comprising a means for decode that is configured to decode the offset adjusted digital signal to provide the digital output signal, wherein the digital output signal is within the full dynamic range.

18. The analog-to-digital converter system of Claim 15, wherein the first means for converting comprises one of a flash-type analog-to-digital converter and pipeline-type analog-to-digital converter.

19. The analog-to-digital converter system of Claim 15, wherein the output range of the overranging analog-to-digital converter includes the full dynamic range, a lower overrange, and an upper overrange, the analog-to-digital converter system is configured for operation from a first reference signal and a second reference signal, wherein the full dynamic range consists of digital codes that are associated with a range of voltages from a first voltage associated with the first reference signal to a second voltage associated with the second reference signal, the lower overrange consists of digital codes that are associated with voltages that are below the second voltage, and the upper overrange consists of digital codes that are associated with voltages that are above the first voltage.

Application No. (if known): 10/623,149 Attorney Docket No.: 08211/0200245-US0

Certificate of Express Mailing Under 37 CFR 1.10

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Airbill No. EV 382054071-US in an envelope addressed to:

MS Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on January 12, 2005
Date

B.W. Lee
Signature

B.W. LEE
Typed or printed name of person signing Certificate

Registration Number, if applicable

Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

Request for Certificate of Correction Pursuant to 37 CFR 1.322 and 37 CFR 1.323 (3 pages)
Certificate of Correction (1 page)
Copies of pages 3, 5, 6, 7, 8, 10, 11, 15 & 16.
Check for $100.00 CK# 7302